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(FOR THE CANDIDATES ADMITTED DURING THE ACADEMIC YEAR 2025 ONLY) 25UDA102

REG.NO. :

N.G.M.COLLEGE (AUTONOMOUS) : POLLACHI

END-OF-SEMESTER EXAMINATIONS : NOVEMBER-2025

BSC CS WITH DA(SF) **MAXIMUM MARKS: 75**

SEMESTER : I **TIME : 3 HOURS**

PART - III

25UDA102 - DIGITAL ELECTRONICS AND COMPUTER ARCHITECTURE

SECTION – A (10 X 1 = 10 MARKS)

ANSWER THE FOLLOWING QUESTIONS. (K1)

1. What is the binary equivalent of the octal number 75?

   a) 111110_2 b) 111101_2 c) 1111011_2 d) 1111101_2

2. In Boolean algebra, A + A' equals:_____

   a) A b) 0 c) 1 d) A'

3. Which flip-flop is free from the race-around condition?

   a) RS Flip-Flop b) JK Flip-Flop c) Master-Slave JK Flip-Flop d) Gated D Flip-Flop

4. Which I/O method requires the CPU to wait until the I/O operation is complete?

   a) Interrupt-driven I/O b) DMA transfer c) Programmed I/O d) Memory-mapped I/O

5. Which type of ROM can be erased using ultraviolet light?

   a) PROM b) EPROM c) EEPROM d) Flash memory

ANSWER THE FOLLOWING IN ONE (OR) TWO SENTENCES (K2)

6. What is the 1's complement of $(101101)_2$?
7. What is the Boolean expression for a two-input NOR gate?
8. Which decoder is used to drive a seven-segment display?
9. Which transfer mode uses a separate control line to signal data readiness?
10. Which memory acts as a buffer between CPU and main memory?

SECTION – B (5 X 5 = 25 MARKS)

ANSWER EITHER (a) OR (b) IN EACH OF THE FOLLOWING QUESTIONS.(K3)

11. a) Convert the decimal number 345 into binary, octal, and hexadecimal formats.

    (OR)

    b) Differentiate between ASCII code and Excess-3 code with examples.

12. a) Draw the logic symbol and truth table for NAND and NOR gates. Explain why they are called universal gates.

    (OR)

    b) State and prove Demorgan's Theorems using truth tables.

(CONT….2)

Ethical paper

13. a) Explain the design procedure of a 4-to-1 multiplexer with logic diagram.

(OR)

b) Explain the operation of an edge-triggered D flip-flop with logic diagram and truth table.

14. a) Describe the different instruction formats with suitable examples.

(OR)

b) Explain the concept of an I/O interface and its importance in system design.

15. a) Draw and explain the memory hierarchy diagram, showing different levels and their characteristics.

(OR)

b) Write short notes on magnetic disks and magnetic tapes.

SECTION – C (5 X 8 = 40 MARKS)

ANSWER EITHER (a) OR (b) IN EACH OF THE FOLLOWING QUESTIONS.(K4 (Or) K5)

16. a) Explain 1's, 2's, 9's, and 10's complements with suitable examples.

(OR)

b) Explain error detection using parity bits and error correction using Hamming code, with suitable examples.

17. a) Draw the truth tables for AND, OR, NOT gates and construct NAND and NOR-only implementations of these gates.

(OR)

b) Explain the procedure for converting a truth table to a Karnaugh map (K-map) and perform simplification using the **SOP method** for the function:
$F(A,B,C,D)=\Sigma(0,1,2,5,6,7,8,9,10,14)$

18. a) Design a full adder using two half adders and an OR gate.

(OR)

b) Explain the operation of a JK Master-Slave Flip-Flop with the help of a neat diagram, truth table, and timing diagram. Discuss how it eliminates the race-around condition.

19. a) Draw and explain the architecture of a general register organization in a CPU and how it supports different addressing modes.

(OR)

b) Discuss different modes of transfer in I/O operations: Programmed I/O, Interrupt-driven I/O, and DMA. Compare their advantages and disadvantages.

20. a) Explain in detail the design and organization of RAM and ROM chips. Include diagrams and examples**.**

(OR)

b) Explain cache mapping techniques: Direct mapping, Associative mapping, and Set-associative mapping, with diagrams.

Ethical paper

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